

FIG. 1 is a block diagram of a system architecture for generating and implementing a system.

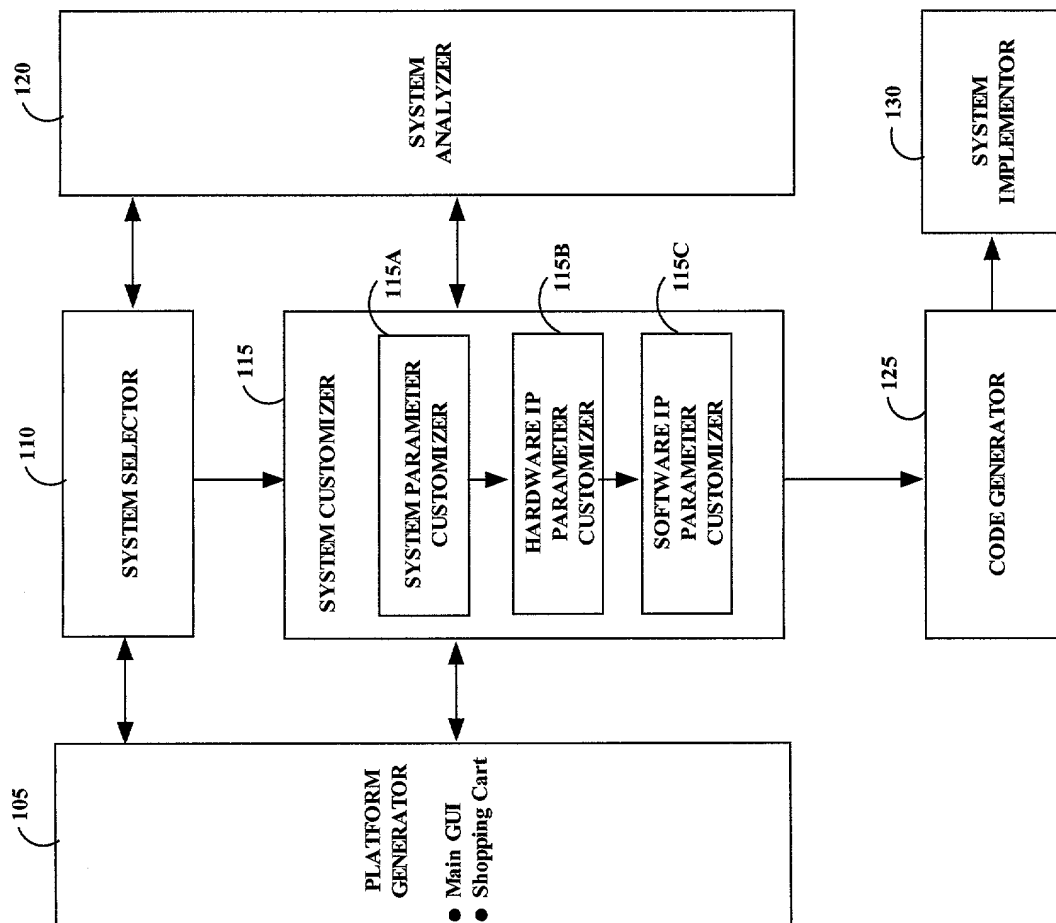


FIG. 1

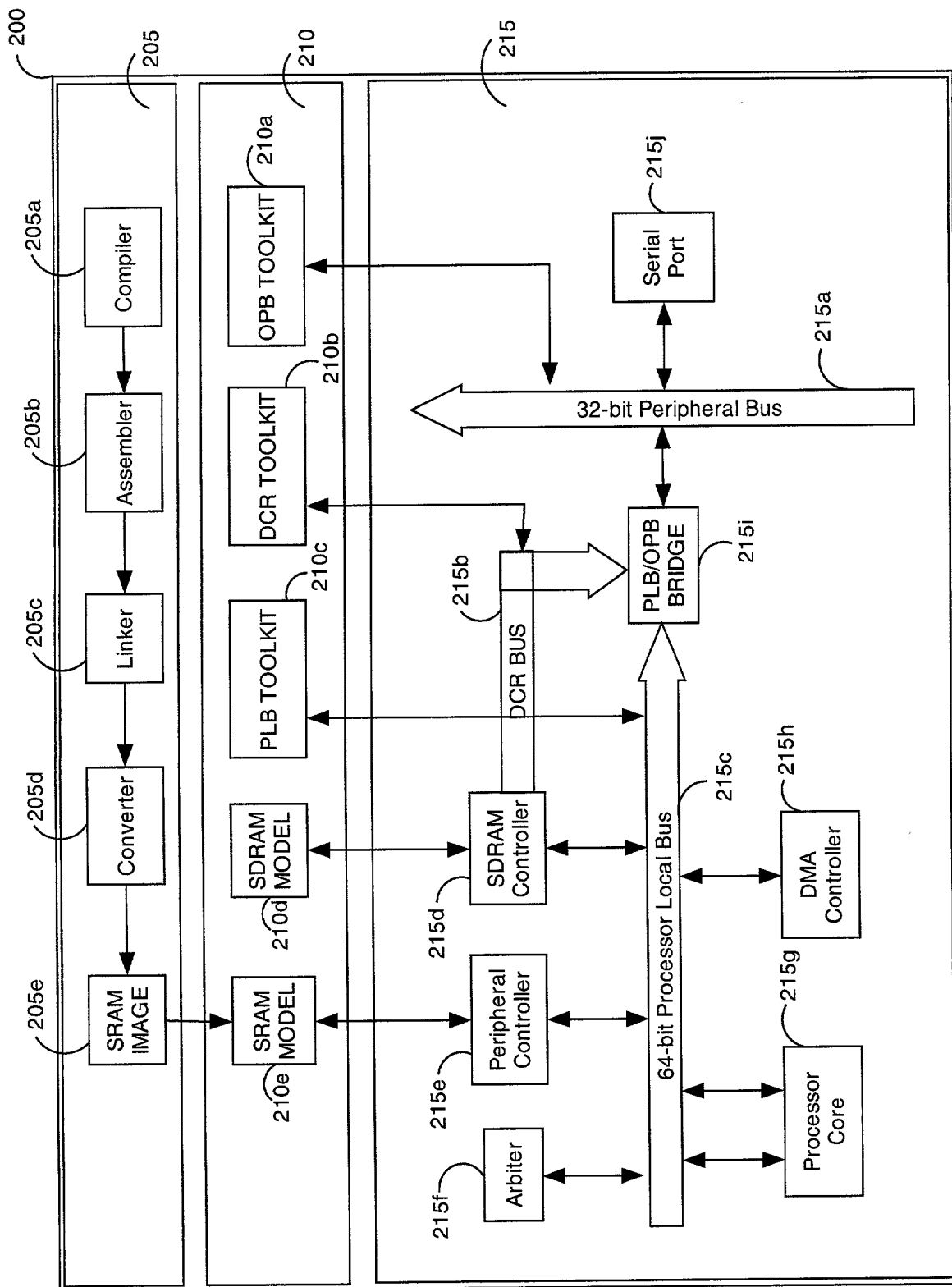


FIG. 2

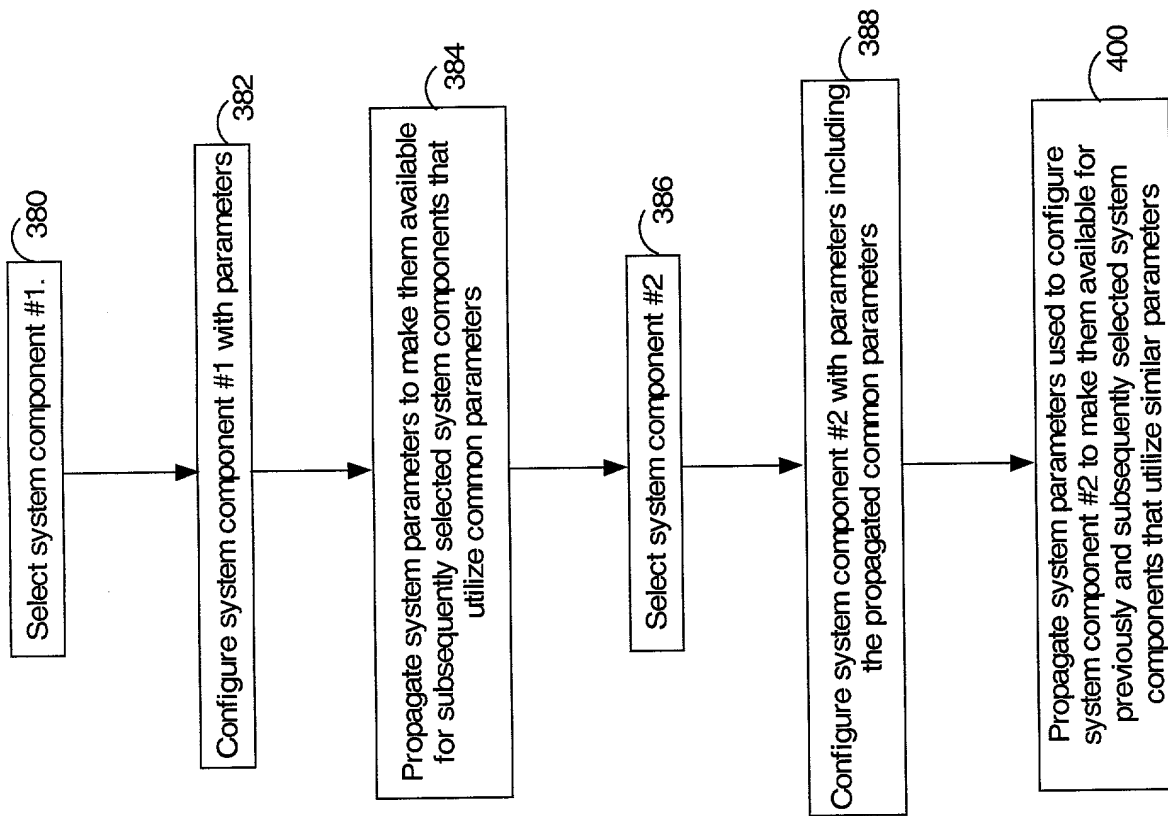


FIG. 3

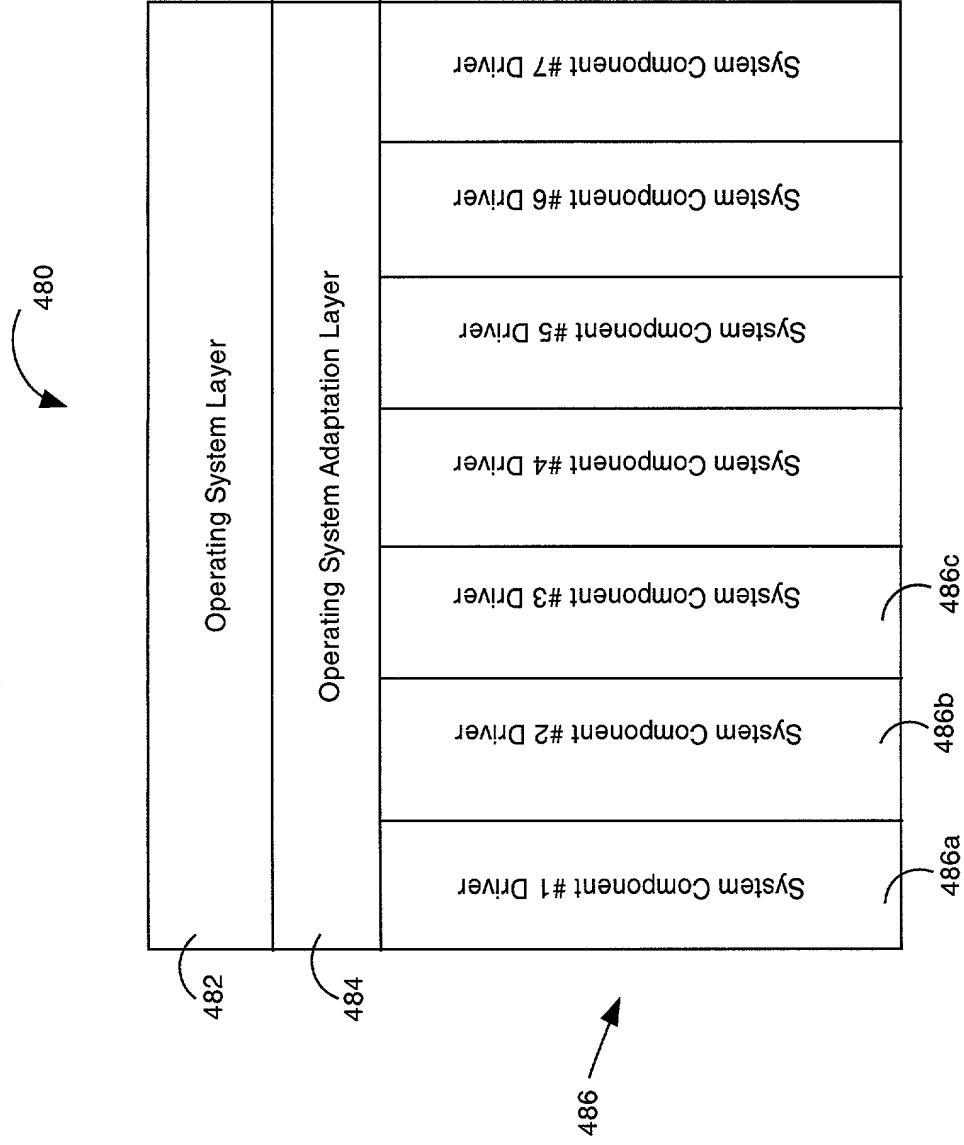


FIG. 4

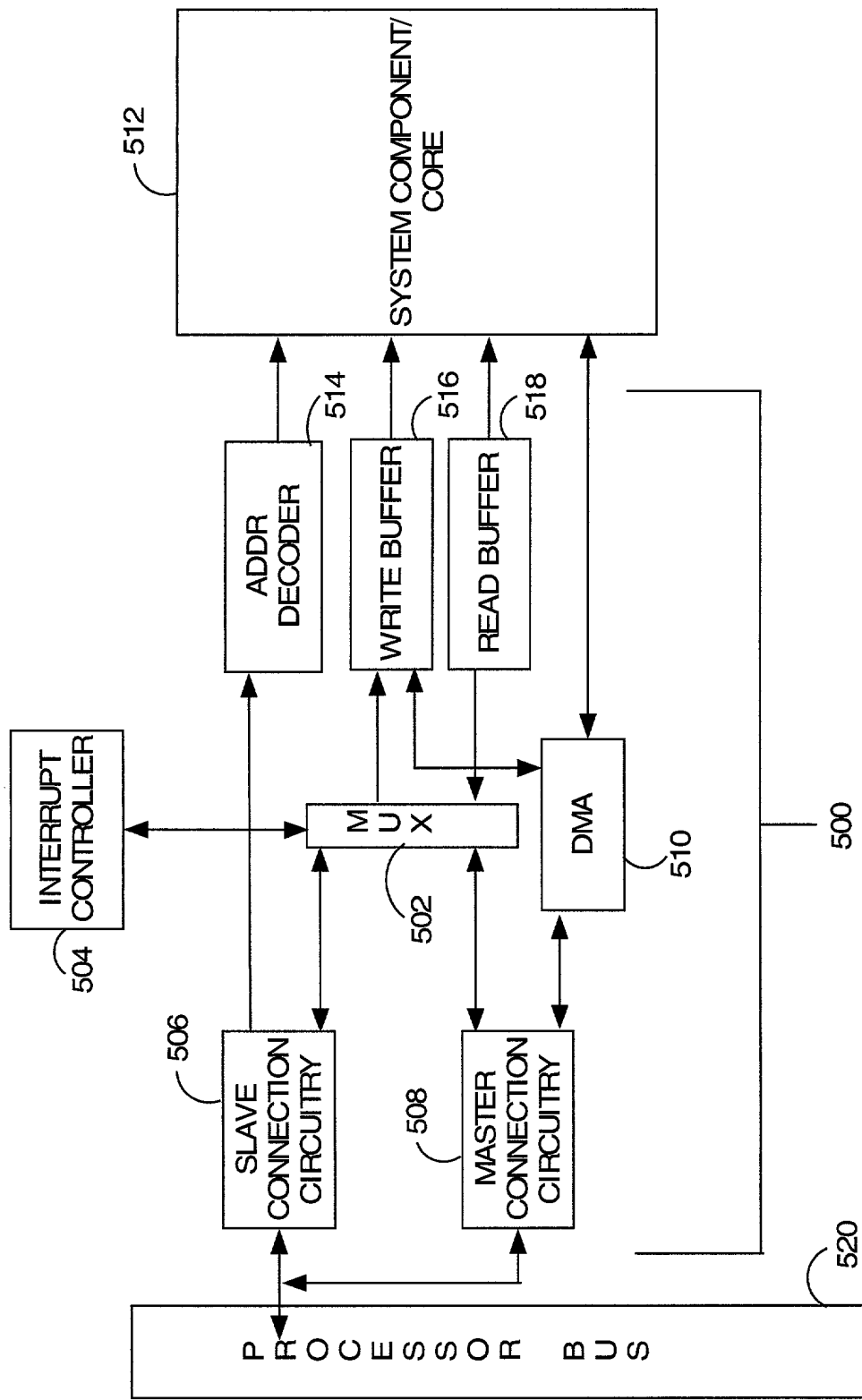


FIG. 5

System Component Selection

☒ OPB Arbiter
 ☒ Ethernet 10/100
 ☒ Ethernet 100/200

☒ UART 16450
 ☒ UART 16550

Parameter Selection

OPB Arbiter

UART 16550

Ethernet 10/100

IRQ 9

354a

Message

Insufficient D-FFs available
 for use by UART 16550
 Alternative Device: UART 16450

Display

DEVICE	LUTs	D-FFs	SLICES	BRAMs	I/Os	MEMORY	PROCESSOR
OPB Arbiter	300	200	200	0	None	1 Kb	0.2 DMIPS
UART 16550	500	121000	300	0	9	2 Kb	1.4 DMIPS
Ether 10/100	2500	1700	1500	0	12	10 Kb	8.4 DMIPS
TOTAL USED	3300	122900	2000	0	21	13 Kb	10 DMIPS
AVAILABLE	122880	122880	61440	3456 K	1488	1000 Kb	300 DMIPS
AVAILABLE	119580	0	59440	3456 K	1267	987 Kb	290 DMIPS

FIG. 6